CRASH COURSE

USN | | | | | | | | | | |

10EE764

Seventh Semester B.E. Degree Examination, May 2017
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Explain the process of nMOS fabrication with neat diagrams. **(10 Marks)**

b. Discuss Moore's law with graph. **(04 Marks)**

c. Compare CMOS and Bipolar technology. **(06 Marks)**

2 a. Define Z_{pu} and Z_{pd} – show that pull-up to pull-down ratio for nMOS inverter driven through another nMOS inverter is $Z_{pu}/Z_{pd} = 4/1$. **(10 Marks)**

b. Explain latch-up phenomenon in p-well CMOS inverter. **(06 Marks)**

c. What is pass transistor? Give an example and write demerit of nMOS pass transistor. **(04 Marks)**

3 a. Explain Lambda based design rules for wires and minimize size transistors. **(10 Marks)**

b. Explain buried and butting contract with neat diagram. **(06 Marks)**

c. Draw the circuit and stick diagram for CMOS inverter. **(04 Marks)**

4 a. Define sheet resistance, square capacitance and delay unit. **(06 Marks)**

b. Write briefly on non-inverting type nMOS super buffer. **(04 Marks)**

c. Calculate the total area capacitance for the multilayered structure shown in Fig. Q4(c), Assume for 5μm technology.

i) Metal 1 to substrate : 0.07×10^{-4} pf/μm^2

ii) Poly silicon to substrate : 0.1×10^{-4} pf/μm^2

iii) Crate to channel : 1×10^{-4}pf/μm^2. **(10 Marks)**

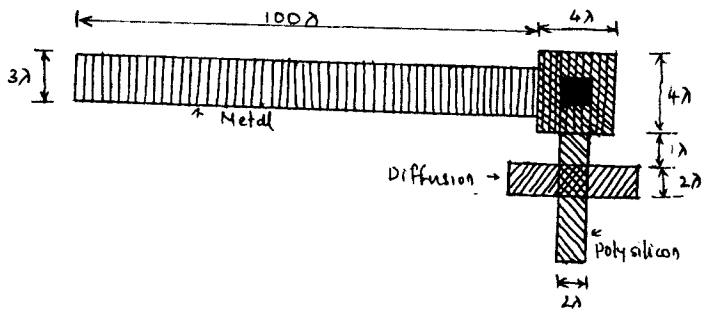

Fig. Q4(c)

PART – B

5 a. What are different scaling models? Explain with neat diagram. **(04 Marks)**

b. Discuss limitations of scaling for interconnect and contact resistance. **(06 Marks)**

c. List any ten scaling factors for device parameters. **(10 Marks)**

6 a. Explain structural design approach for parity generator and draw the nMOS stick diagram of its basic cell. **(10 Marks)**

b. What are the guidelines for a subsystem design process? **(06 Marks)**

c. Write short note on dynamic CMOS logic. **(04 Marks)**

7 a. Explain the operation of 4×4 barrel shifter. **(10 Marks)**

b. Explain the general arrangement of 4-bit arithmetic processor. **(06 Marks)**

c. List the general considerations for VLSI design. **(04 Marks)**

8 a. Show how arithmetic and logical functions are implemented using adder cell. **(10 Marks)**

b. Explain some observations to design process. **(06 Marks)**

c. What is regularity? Explain. **(04 Marks)**

* * * * *